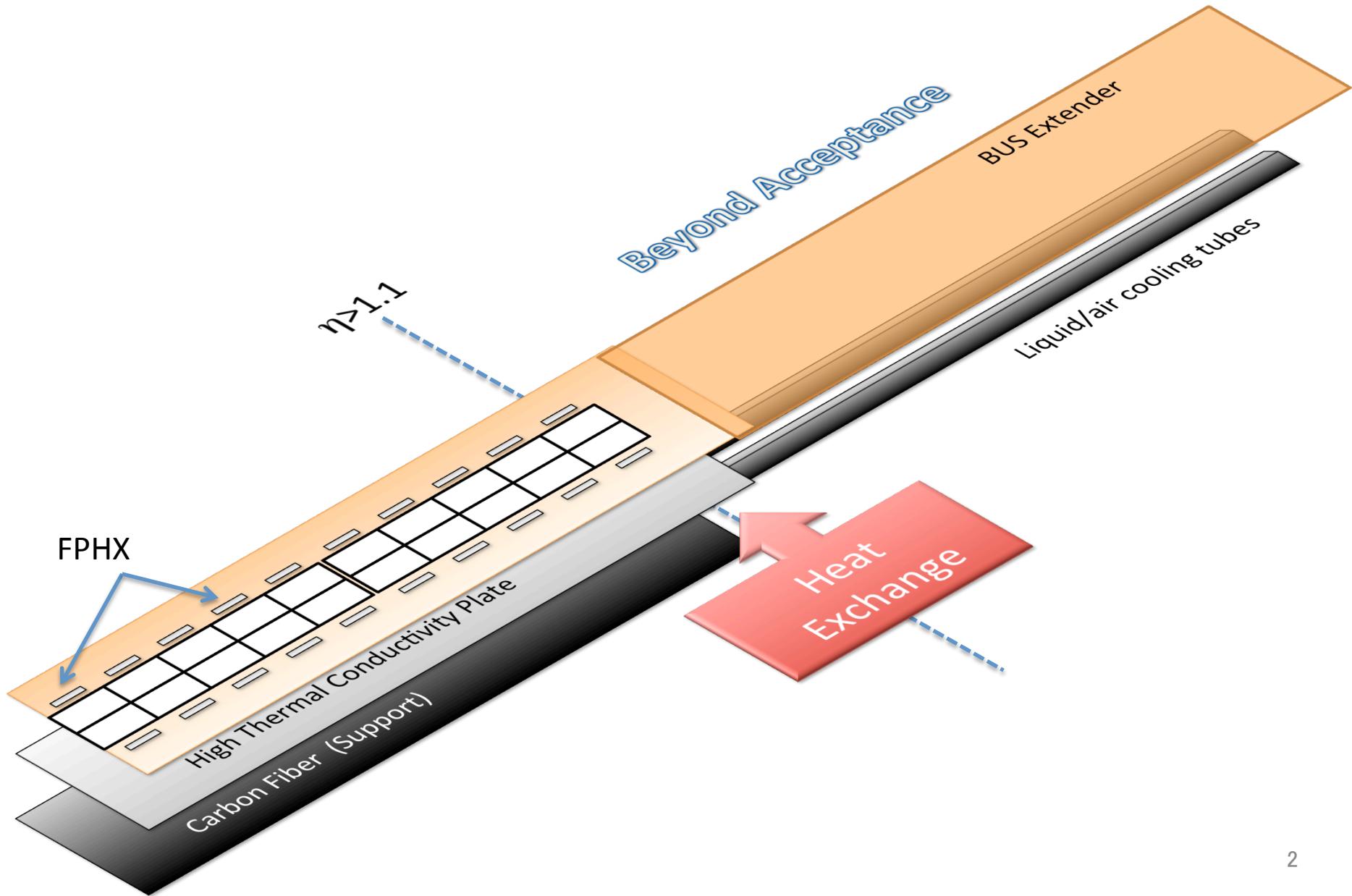


INTT Material Budget Plan

RIKEN/RBRC

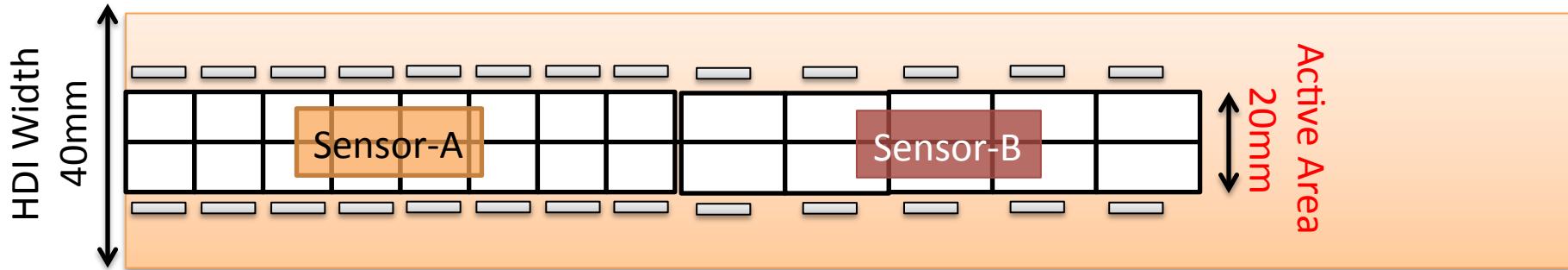
Itaru Nakagawa

Ladder Structure

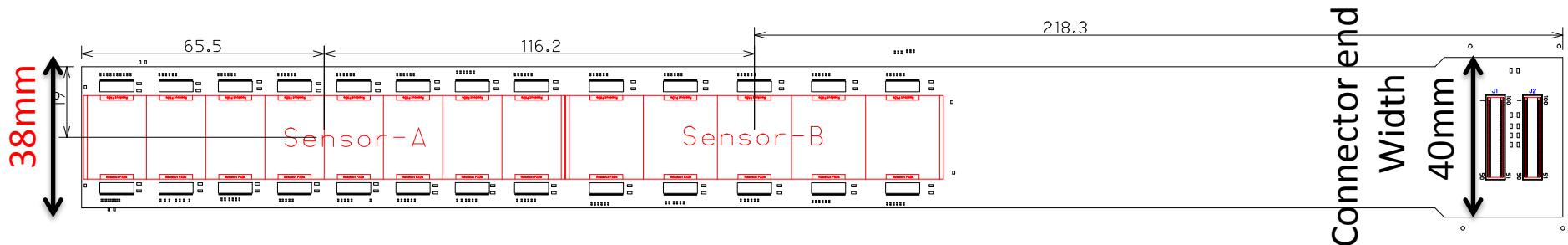


Silicon Module

- Present INTT GEANT Model

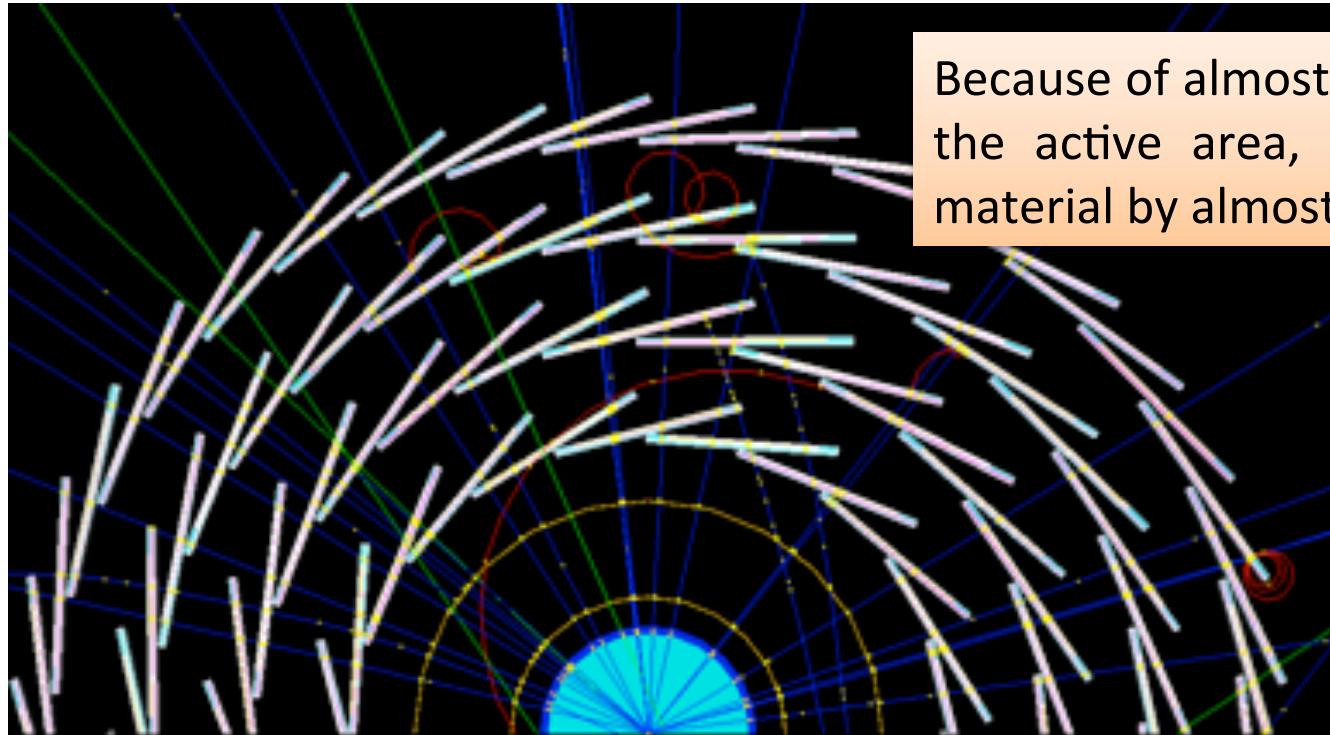


- Prototype Design

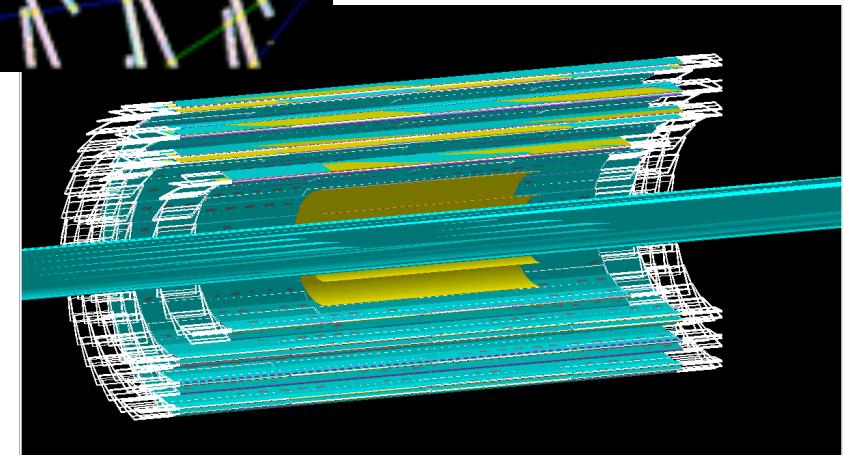


The 38mm is the technological limit width. It is unlikely this width becomes narrower in the future R&D.

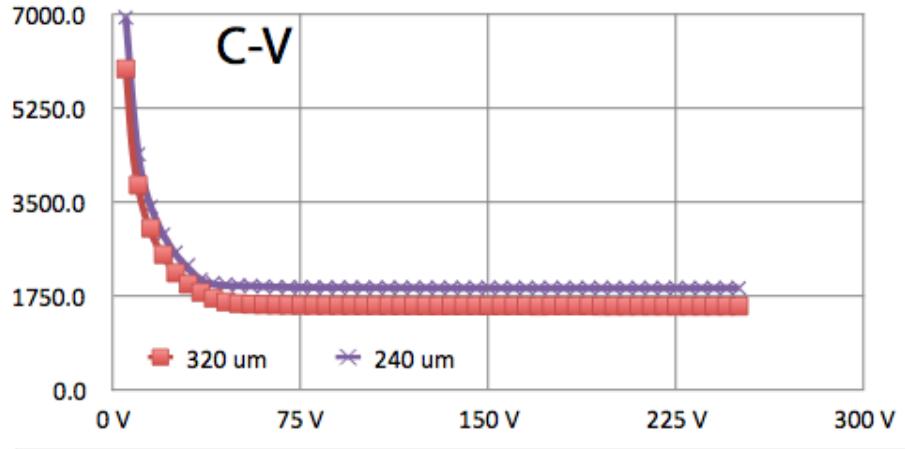
INTT Barrel and Ladder Overlap



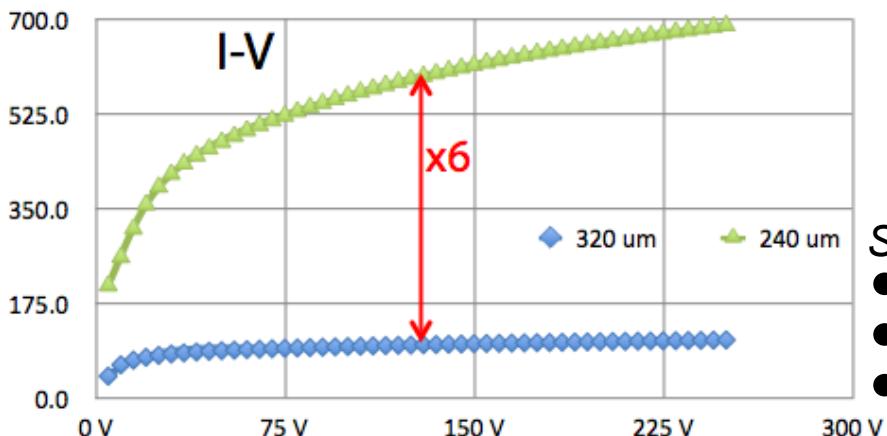
Because of almost factor of 2 wider HDI than the active area, the overlap adds up the material by almost factor of 2.



Reducing Material (Silicon sensors)



Thickness	320 mm	240 mm
Full Depletion Voltage [V]	45	< 45



	R&D Goal	Standard
Thickness	200 μm	240 μm
X0	0.21%	0.26%
Dark current / 320 μm	similar with 240 μm	x6
Price	> 0.5k USD?	0.4k USD
		x1

Silicon sensors for the strip layers

- Two thicknesses, 240 μm and 320 μm .
- 240 μm sensor is made by grinding 320 μm one.
- Hamamatsu says 200 μm is possible.
→ compromise with increasing dark current.

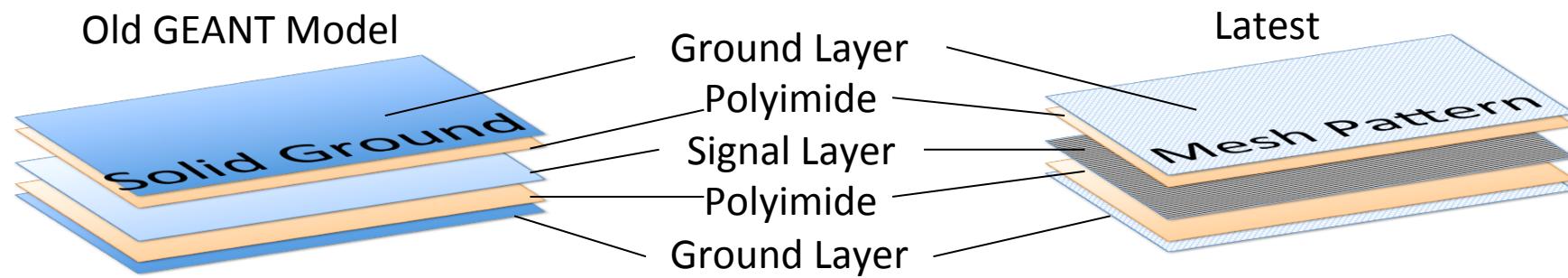
INTT Ladder New Material Budget

	Previous		New	
	Thickness	X/X ₀	Thickness	X/X ₀
Silicon	240 µm	0.3 %	200 µm	0.21%
HDI*	473 µm	0.7 %	473 µm	0.37%
High Thermal Conductivity Plate	350 µm	0.18 %	210 µm	0.10%
Carbon Fiber Support	230 µm	0.08 %	230 µm	0.08%
Total	1293 µm	1.26 %	1113 µm	0.76%

*X/X_{rad} is multiplied by 2 for overlapping ladder. Thus the radiation length is evaluated per active area per ladder.

Modified GEANT Model (HDI)

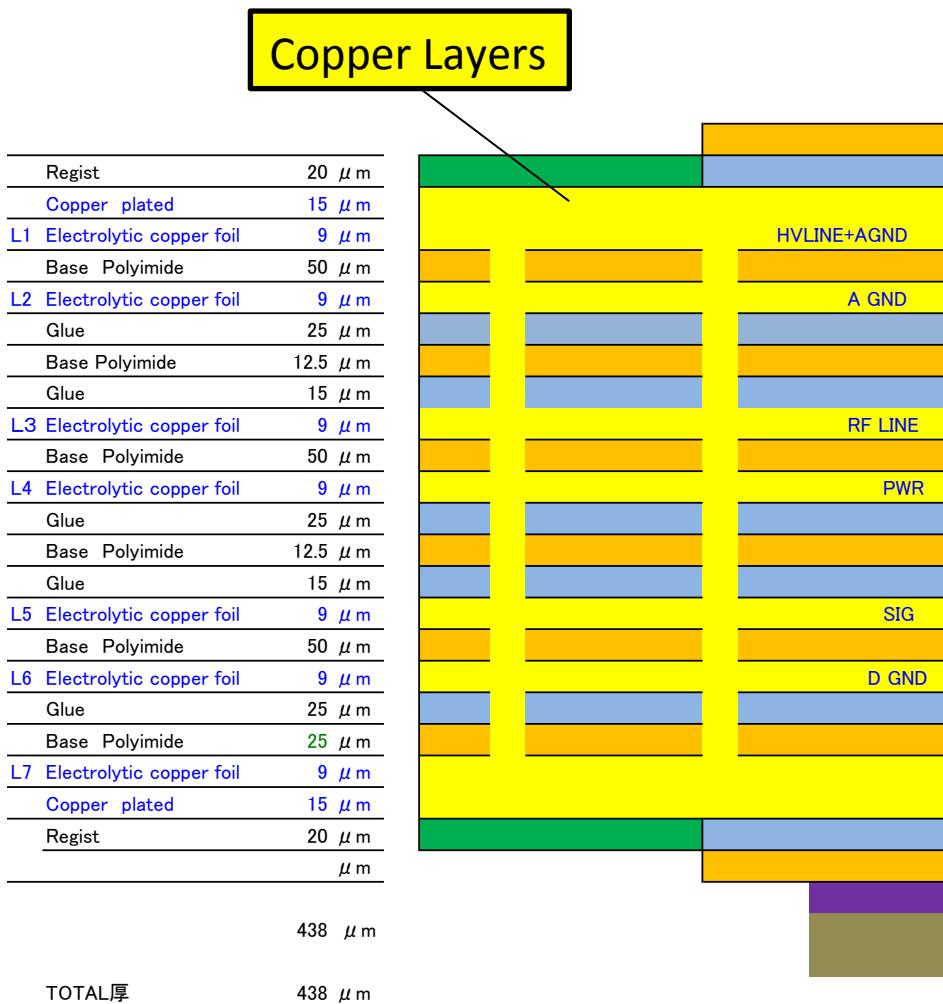
	GEANT Model	Effective Thickness	x/x_{rad} [%]
Copper Layer Total	93 μm	6.26 μm	0.044
Polyimide Total	380 μm	380 μm	0.14
HDI Total			0.184 [%]



All copper layers were assumed to be solid plates in the GEANT model.

Introduced mesh patterns for HV, GND layers, also estimated copper occupancy of the signal layers.

HDI Layer Structure (New)

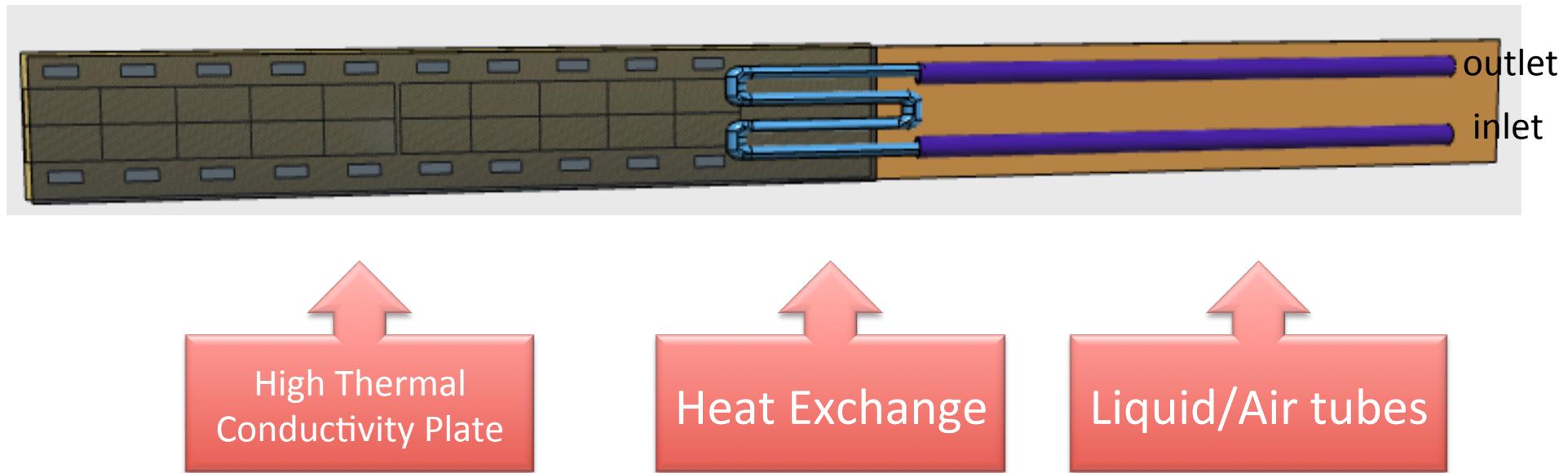


	Sub Component Thickness		
	Copper Layers	Else	
Occupancy	Effective [μ m]	Real [μ m]	[μ m]
Coverlay Polyide	12.5 μm		12.5
Coverlay Glue	25 μm		25
Copper plated	15 μm	10% 1.50	15
L1 Electrolytic copper foil	9 μm	10% 0.90	9
Base Polyimide	50 μm		50
L2 Electrolytic copper foil	9 μm	10% 0.90	9
Glue	25 μm		25
Base Polyimide	12.5 μm		12.5
Glue	15 μm		15
L3 Electrolytic copper foil	9 μm	8.2% 0.74	9
Base Polyimide	50 μm		50
L4 Electrolytic copper foil	9 μm	10% 0.90	9
Glue	25 μm		25
Base Polyimide	12.5 μm		12.5
Glue	15 μm		15
L5 Electrolytic copper foil	9 μm	3.2% 0.29	9
Base Polyimide	50 μm		50
L6 Electrolytic copper foil	9 μm	10% 0.90	9
Glue	25 μm		25
Base Polyimide	25 μm		25
L7 Electrolytic copper foil	9 μm	0.5% 0.05	9
Copper plated	15 μm	1% 0.08	15
Coverlay Glue	25 μm		25
Coverlay Polyimide	12.5 μm		12.5
Glue for support plate	40 μm		
Support Plate FR-4 1.0t	1000 μm		

TOTAL厚	473 μm	Total	6.246	93	380
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Reducing Material : High Thermal Conductivity Plate

- View from the back



The point of high thermal conductivity plate is to transport the heat from the chip to the heat exchange. Carbon fiber support is not drawn here for visibility.

Cooling Option

- In addition to air cooling option, the high thermal conductivity plate (sheet) will be tested. It has an advantage to make the cooling system even simpler and less material.

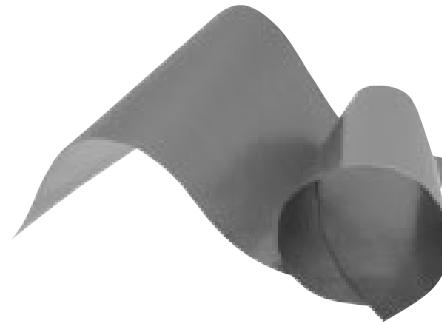
Panasonic

“PGS” Graphite Sheets

“PGS” Graphite Sheets

Type: **EYG**

PGS (Pyrolytic Graphite Sheet) is a thermal interface material which is very thin, synthetically made, has high thermal conductivity, and is made from a highly oriented graphite polymer film. It is ideal for providing thermal management/heat-sinking in limited spaces or to provide supplemental heat-sinking in addition to conventional means. This material is flexible and can be cut into customizable shapes.



■ Characteristics

Characteristics		Specification	Specification	Specification
Thickness		0.10 ± 0.03 mm	0.07 ± 0.015 mm	0.025 ± 0.010 mm
Density		0.85 g/cm ³	1.1 g/cm ³	2.1 g/cm ³
Thermal conductivity	a-b plane	600 to 800 W/(m·K)	750 to 950 W/(m·K)	1500 to 1700 W/(m·K)
Electrical conductivity		10000 S/cm	10000 S/cm	20000 S/cm
Extensional strength		19.6 MPa	22.0 MPa	30.0 MPa
Expansion coefficient	a-b plane	9.3 × 10 ⁻⁷ 1/K	9.3 × 10 ⁻⁷ 1/K	9.3 × 10 ⁻⁷ 1/K
	c axis	3.2 × 10 ⁻⁵ 1/K	3.2 × 10 ⁻⁵ 1/K	3.2 × 10 ⁻⁵ 1/K
Heat resistance		400 °C		
Bending(angle 180,R5)		10000 cycles		

Design and specifications are each subject to change without notice. Ask factory for the current technical specifications before purchase and/or use.
Should a safety concern arise regarding this product, please be sure to contact us immediately.

00 Sep. 2008

Some sample sheets are delivered.

10

Sample Graphite Sheets

- We have graphite sheets to be tested from 3 different companies.

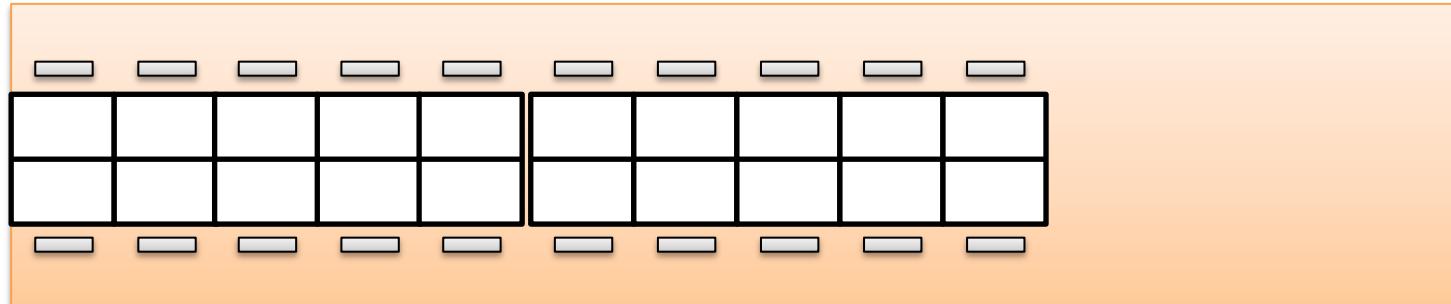
Make	Panasonic	Kaneka	Blady
Thickness [μm]	70	40	70
Thermal Conductivity [Wm/K]	1000	500	300 ~ 1500



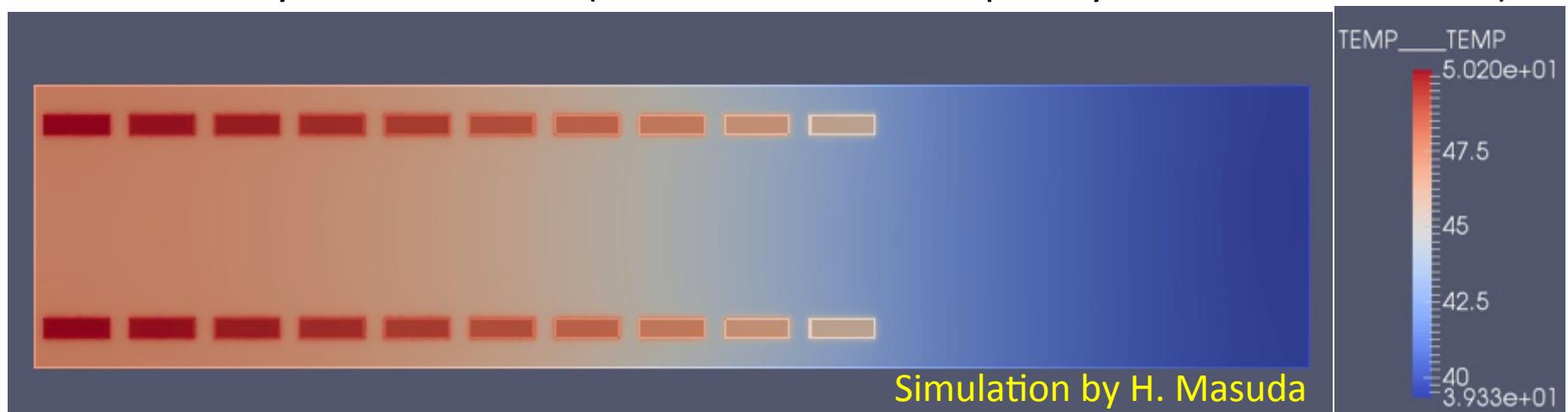
Dimension is made to be same with s0 HDIs (30cm x 4cm x 70 μm)

Cooling Simulation

Layer-0



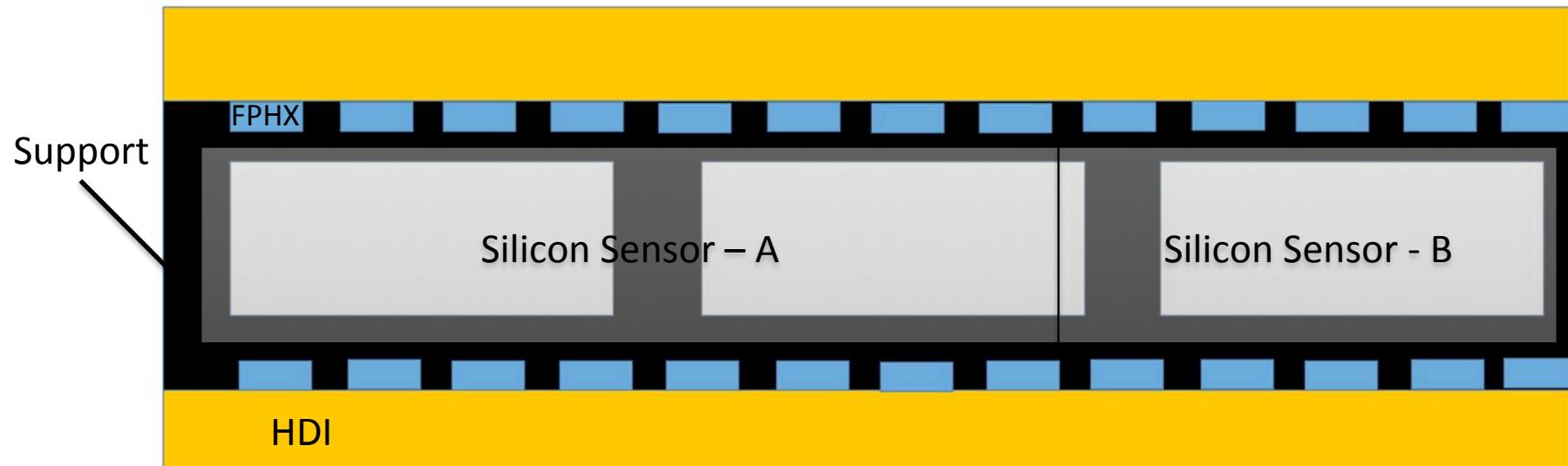
- Predicted by the Simulation (Salome-meca Developed by Electricite De France)



Condition: FPHX 65mW/chip, 70 μ m Graphite Sheet (1200W/mK), 100% longitudinal heat transfer is assumed. Still need a fine tuning.

Reducing Material : Support

- Do we need to backup entire silicon acceptance or can it be open behind silicon sensors?



To be studied with engineers.

Improving Reconstruction Algorithm

Work by Gaku Mitsuka

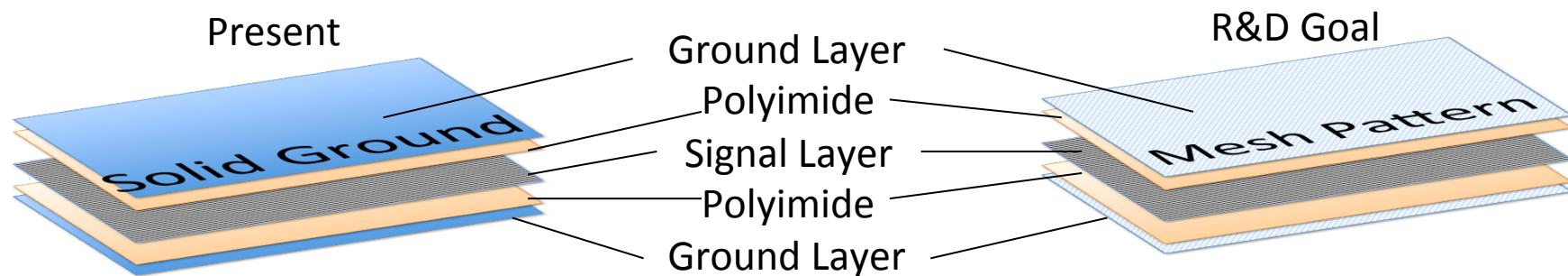
- Alan's code does Hough transform for all MAPS, INTT, TPC. (Ignores multiple scattering effect).
- Step-1 (by mid Feb.) Hough transform only for TPC. Tracklet reconstruction by TPC only.
- Step-2 (by mid. March) Develop the algorithm to start from inner TPC tracklet to find relevant hit in INTT and MAPS. Search window reflects the multiple scattering effect.

Summary

- Due to the technical limit of HDI width, the ladder overlap between ladder will adds up material by factor of 2.
- HDI width is 38mm and unlikely to be narrower in future R&D.
- R&Ds are in progress for each components of ladders.
- Algorithm is under development to improve the tracking which makes the tracker material less impactful to the momentum resolution by taking into account the multiple scattering effect in the hit search window.

BACKUP

Reducing Material (HDI)



Signal layers are electrically shielded by sandwiched by solid ground layers

solid ground layers are meshed pattern so that to reduce material without loosing noise shielding performance. The goal is to reduce the Cu material by 10%. (Prototype is to be delivered in April)

Material	X/X ₀	R&D Goal
Polyimide Total	0.3 %	
Copper Layer Total	0.4 %	0.04 %

INTT Ladder Material Budget

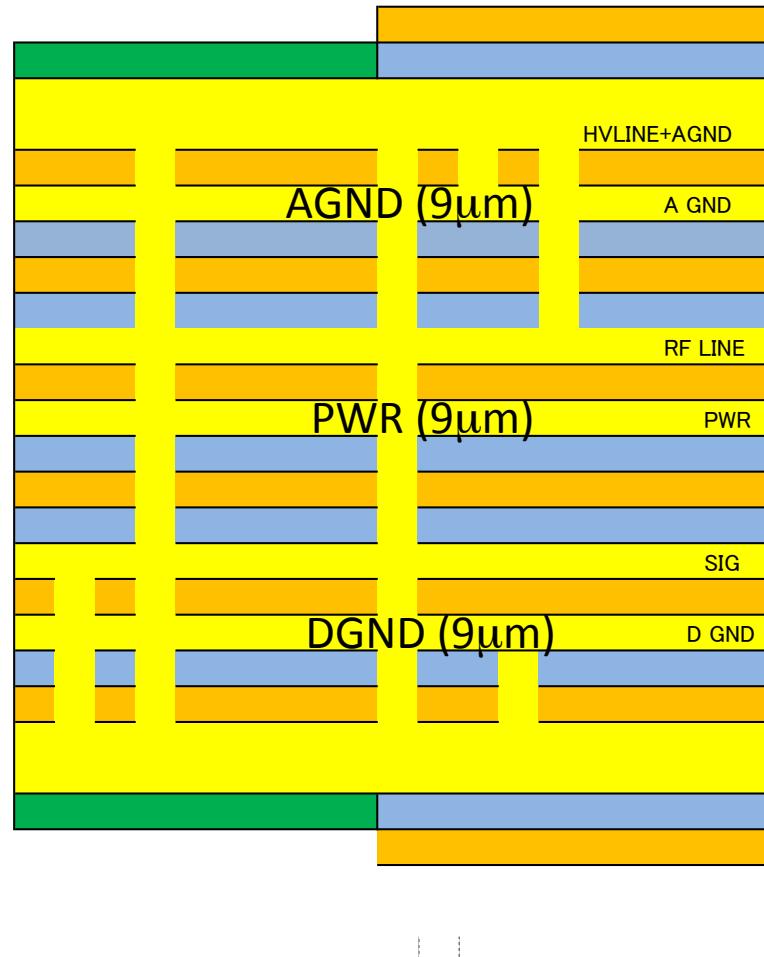
	Thickness	Radiation Length X/X_0	R & D Goal
Silicon	240 μm	0.3 %	0.25 ~ 0.3 %
HDI*	< 500 μm	0.7 %	0.34 ~ 0.7%
High Thermal Conductivity Plate	350 μm	0.18 %	0.09? ~ 0.18 %
Carbon Fiber Support	230 μm	0.08 %	0.05? ~ 0.08%
Total		1.26 %	0.73? ~ 1.26%

* X/X_0 is multiplied by 2 for overlapping ladder

HDI Layer Structure (old)

Regist	20 μm
Copper plated	15 μm
L1 Electrolytic copper foi	9 μm
Base Polyimide	50 μm
L2 Electrolytic copper foi	9 μm
Glue	15
Coverlay Polymide	12.5 μm
Glue	25 μm
L3 Electrolytic copper foi	9 μm
Base Polyimide	50 μm
L4 Electrolytic copper foi	9 μm
Glue	15 μm
Coverlay Polymide	12.5 μm
Glue	25 μm
L5 Electrolytic copper foi	9 μm
Base Polyimide	25 μm
L6 Electrolytic copper foi	9 μm
Bonding Sheet	25 μm
Base Polyimide	50 μm
L7 Electrolytic copper foi	9 μm
Copper plated	15 μm
Regist	20 μm
μm	

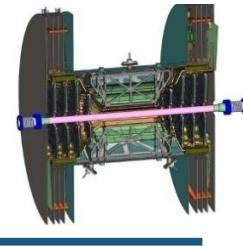
438 μm



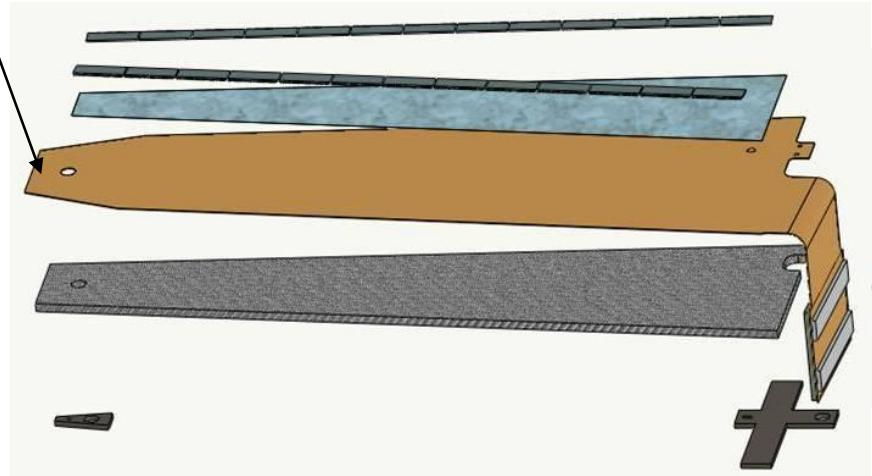
Coverlay Polyimide	12.5 μm
Coverlay Glue	25 μm
Copper plated	15 μm
L1 Electrolytic copper foil	9 μm
Base Polyimide	50 μm
L2 Electrolytic copper foil	9 μm
Glue	15 μm
Coverlay Polyimide	12.5 μm
Glue	25 μm
L3 Electrolytic copper foil	9 μm
Base Polyimide	50 μm
L4 Electrolytic copper foil	9 μm
Glue	15 μm
Coverlay Polyimide	12.5 μm
Glue	25 μm
L5 Electrolytic copper foil	9 μm
Base Polyimide	25 μm
L6 Electrolytic copper foil	9 μm
Bonding Sheet	25 μm
Base Polyimide	50 μm
L7 Electrolytic copper foil	9 μm
Copper plated	15
Coverlay Glue	25 μm
Coverlay Polyimide	12.5 μm
TOTAL Thickness	
473 μm	

TOTAL Thickness	Material	X/X ₀	R&D Goal
	Polyimide Total	0.3 %	
	Copper Layer Total	0.4 %	0.044%

fVTX Prototype HDI Wedge Assembly (Nov. 08)



HDI



HDI trace count

2 R/O lines x LVDS pair x 26 chips	104	100Ω impedance
4 Download and Reset lines	4	100Ω impedance
2 Clocks x LVDS pair	4	100Ω impedance
1 Calibration line	1	50Ω impedance
	113	

- **High Density Interconnect (HDI) – kapton flat cable to supply bias to sensor and power to FPHX chips, and transfer data from the chips to the read-out electronics**
 - ~440µm thick
 - 7 copper planes, 6 Kapton films
 - Thickness/Rad length = 0.00425

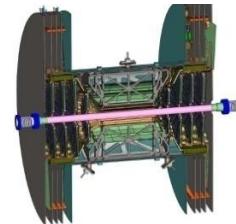
~0.4% by HDI only

WBS 1.4.3

fVTX Prototype HDI Layer Thickness and Radiation Thickness

(Total thickness)/(Radiation length):

0.00419



Radiation lengths (cm) of Layers:		copper:	1.43	kapton:	28.6	epoxy:	44.37	
	#of layers	fraction of layers	thickness (μm)	R_L	thickness (μm)	Production	Imp target	Ref plane (layer)
top covercoat	1	0.2	38	0.171287	10	10		
copper 1	1	0.8	12	6.713287	25	18	50 SE	2
kapton 1	1	1	25	0.874126	25	20		
epoxy 1	1	1	12	0.270453	12	15		
copper 2	1	0.9	12	7.552448	12	11		
kapton 2	1	1	40	1.398601	25	20		
epoxy 2	1	1	12	0.270453	12	15		
copper 3	1	0.1	12	0.839161	12	9	100 DIFF	2,4
kapton 3	1	1	50	1.748252	50	50		
copper 4	1	0.9	12	7.552448	12	11		
epoxy 3	1	1	12	0.270453	12	15		
kapton 4	1	1	40	1.398601	25	20		
copper 5	1	0.1	12	0.839161	12	11	100 DIFF	2,4
epoxy 4	1	1	12	0.270453	12	15		
kapton 5	1	1	40	1.398601	25	20		
copper 6	1	0.9	12	7.552448	12	11		
epoxy 5	1	1	12	0.270453	12	15		
kapton 6	1	1	25	0.874126	25	20		
copper 7	1	0.2	12	1.678322	25	18	50 SE	6
bottom covercoat	1	0.7	38	0.599504	10			
Total thickness (μm) of HDI:			440	42.54264	365	10	334	



Douglas Fields, fVTX HDI Technical Review
October 23, 2009



The University of New Mexico

Silicon Module with Liquid/Air cooling Design

